

FIG. 1 (PRIOR ART)

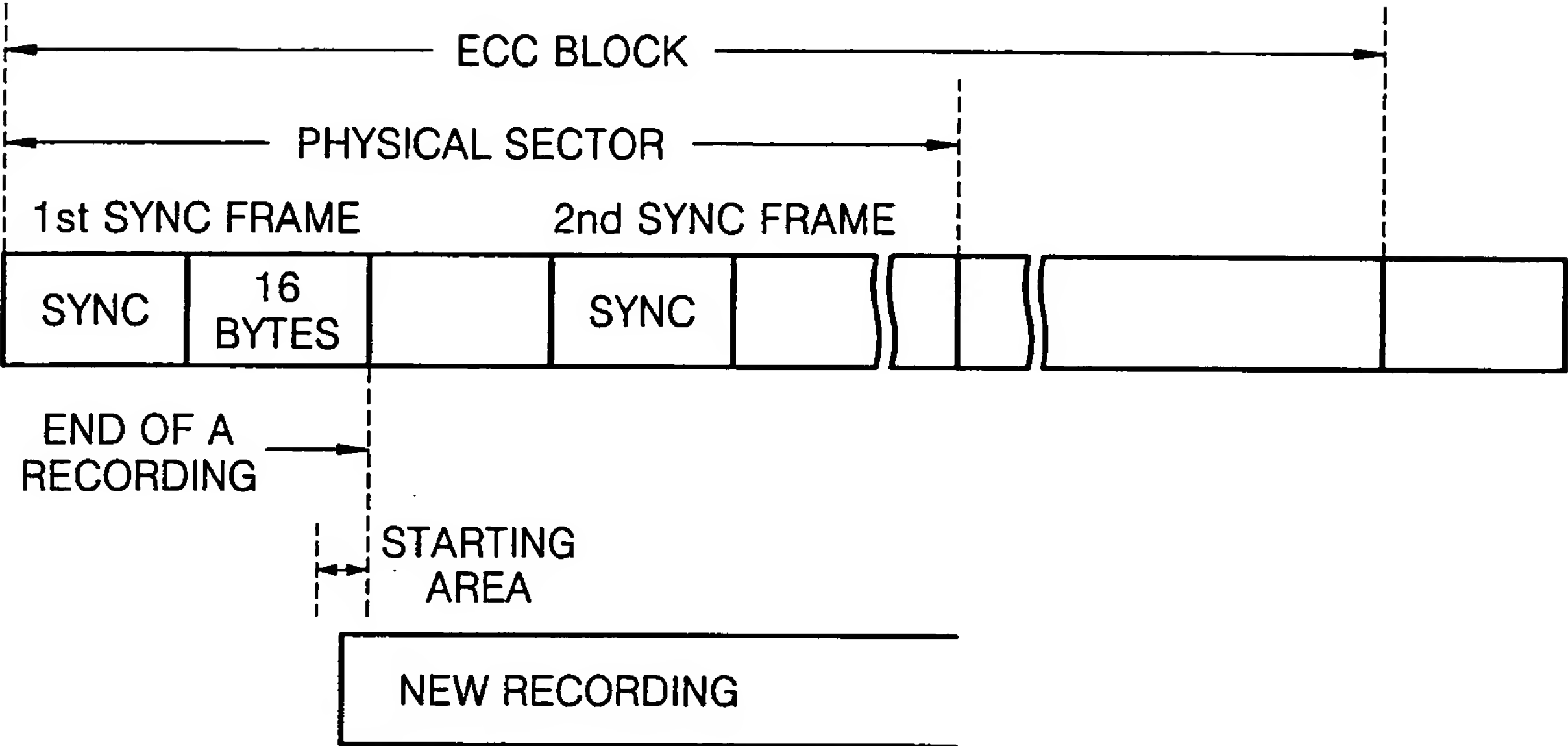
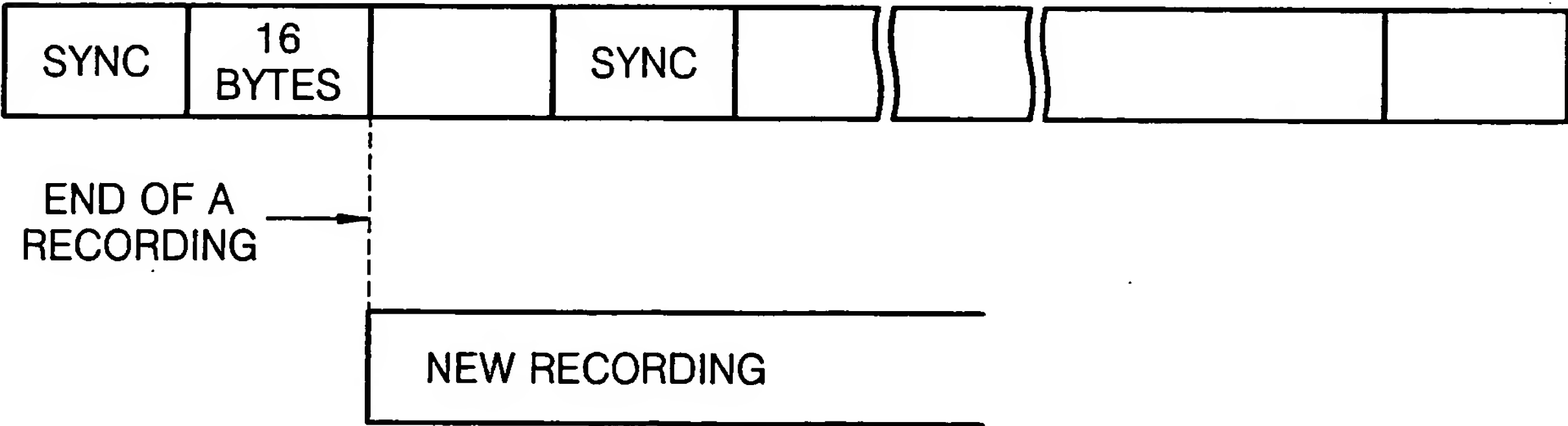


FIG. 2 (PRIOR ART)



< NO ERROR >

FIG. 3 (PRIOR ART)

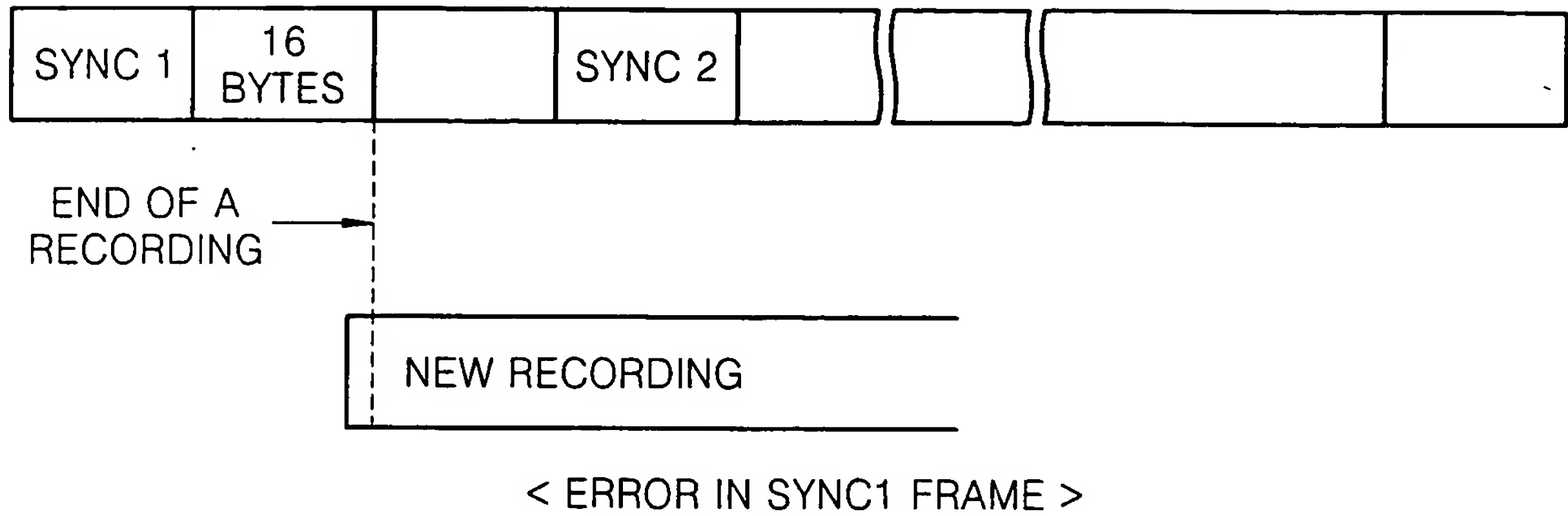


FIG. 4 (PRIOR ART)

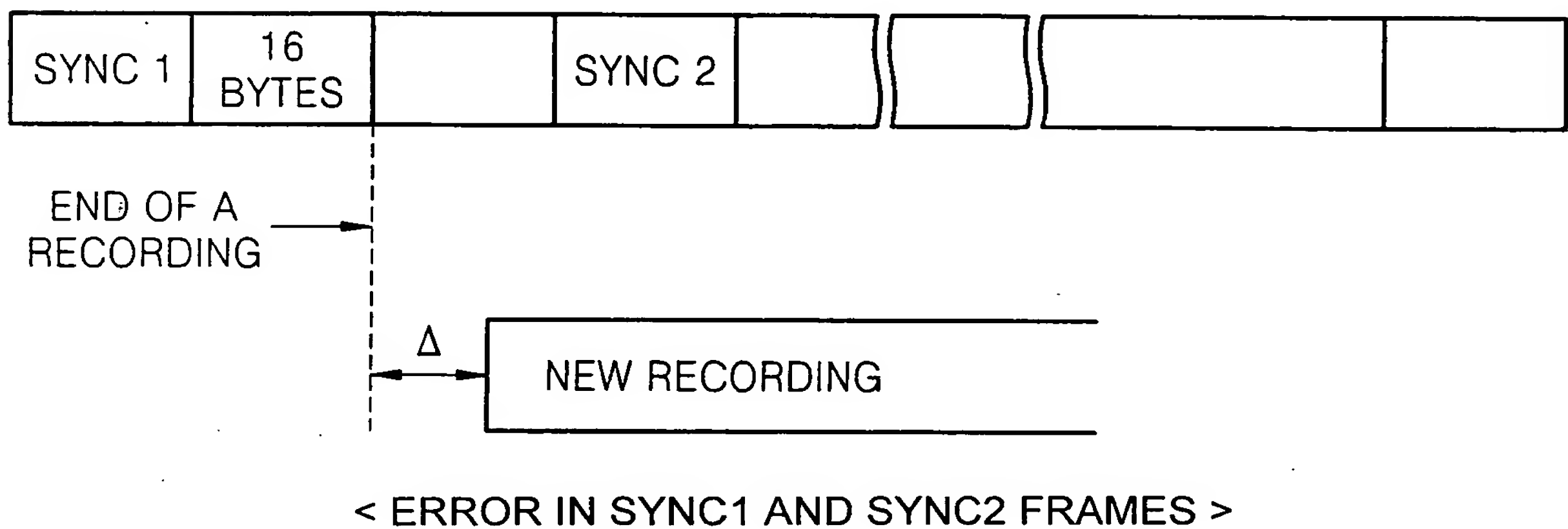


FIG. 5

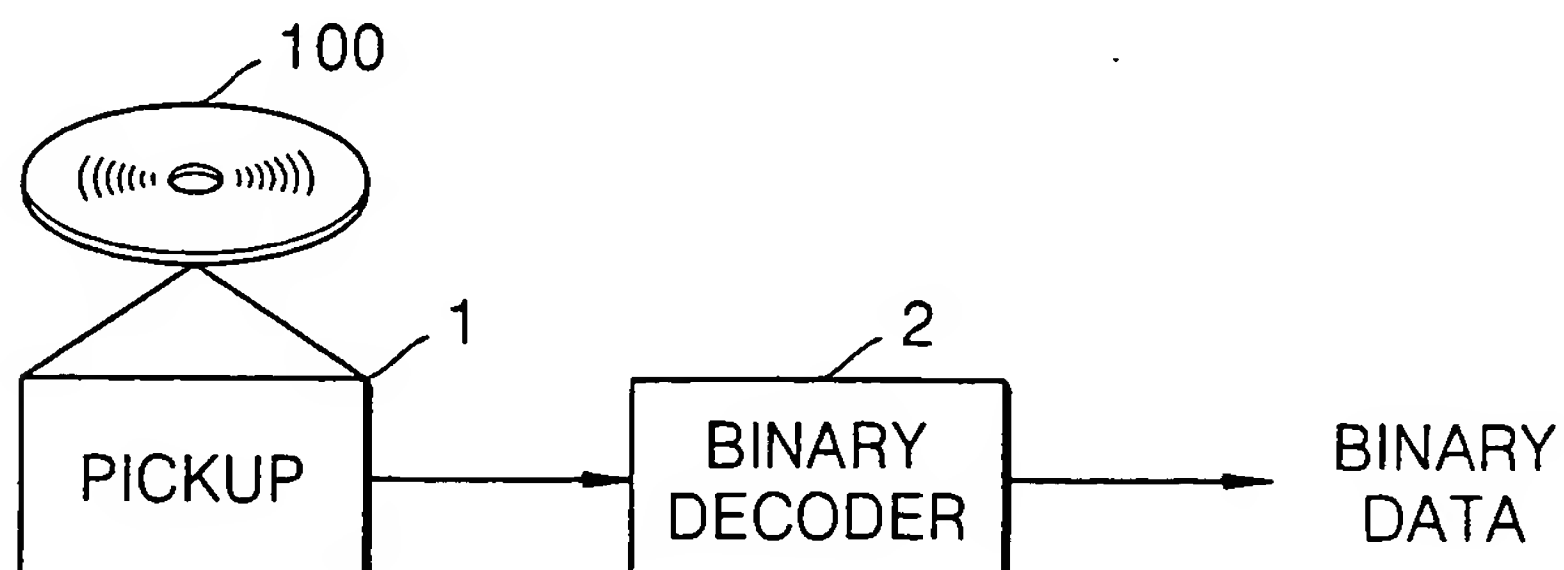


FIG. 6

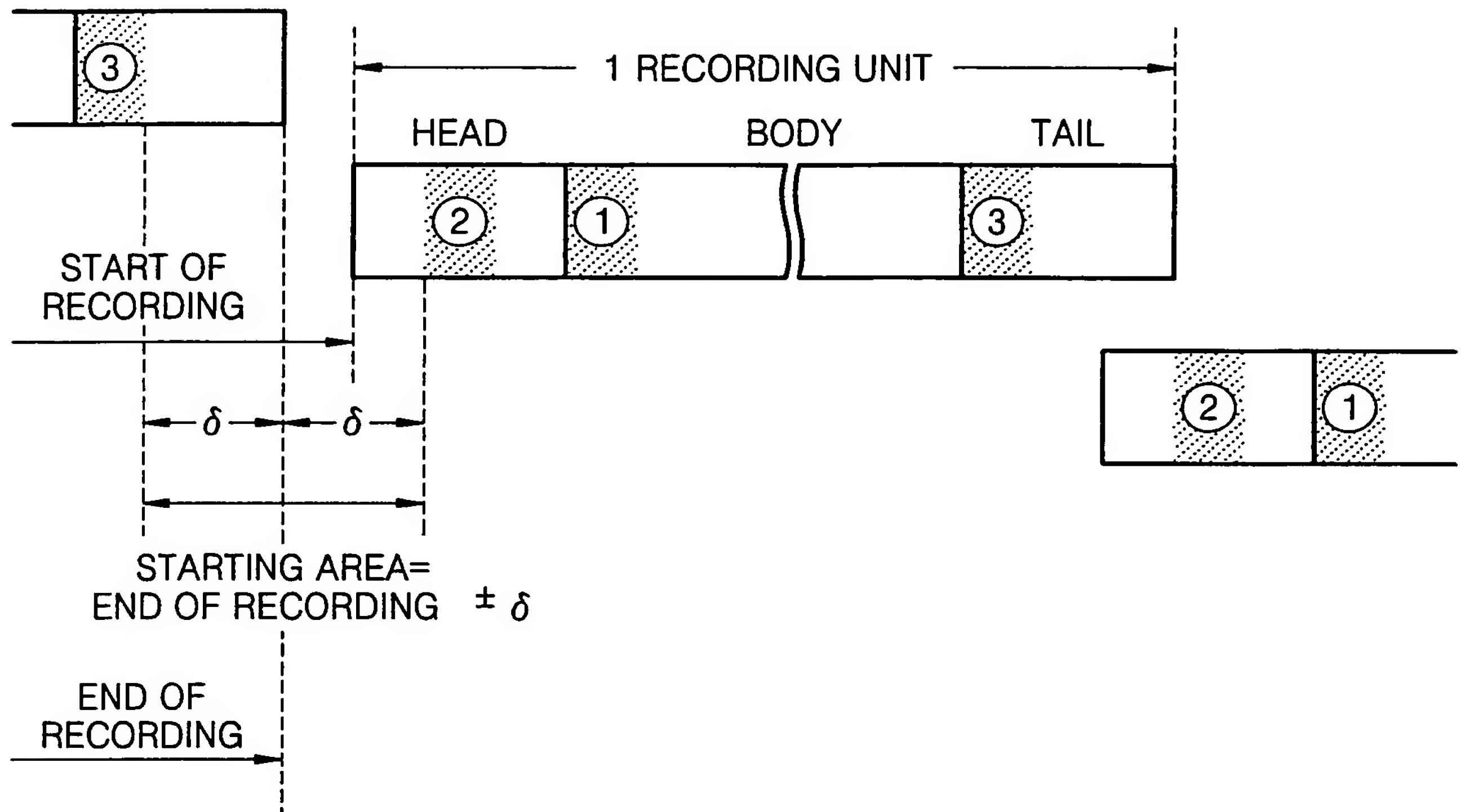


FIG. 7

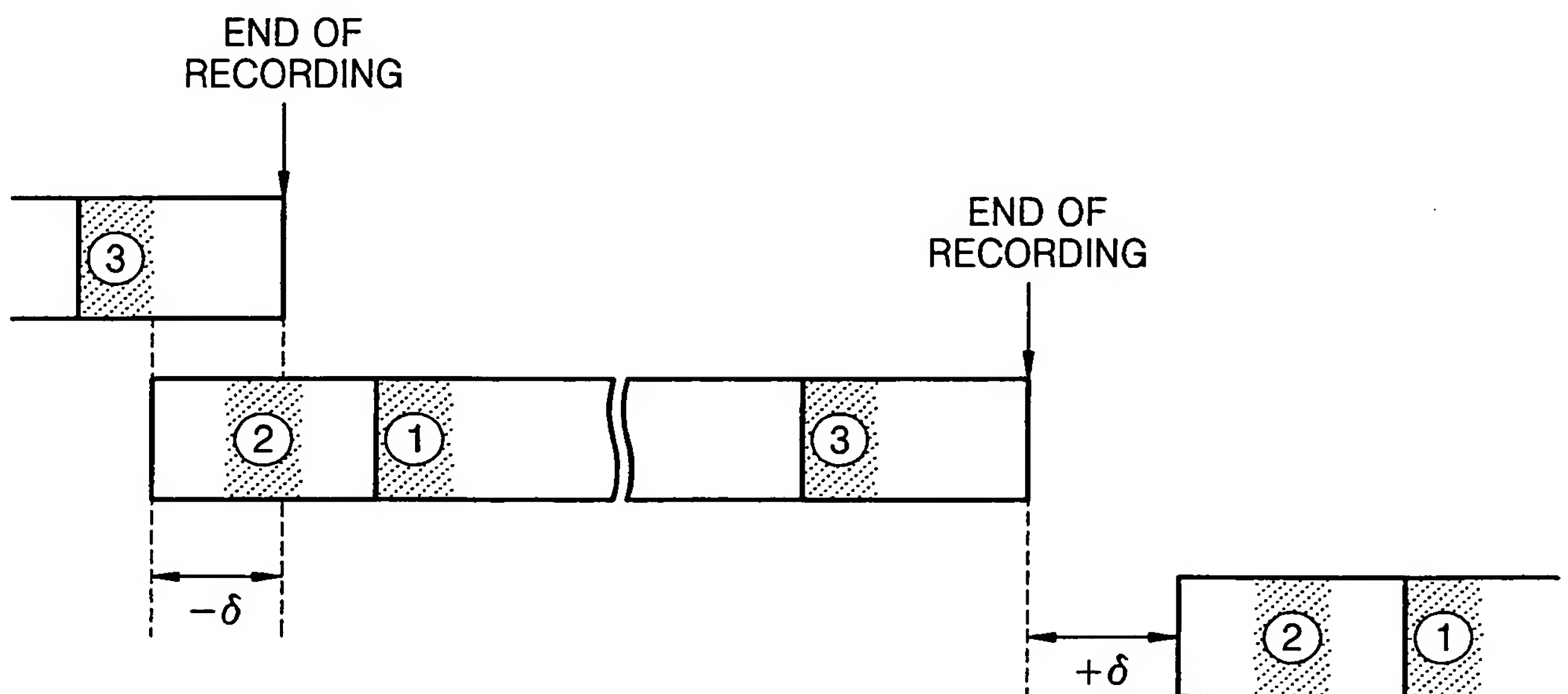


FIG. 8

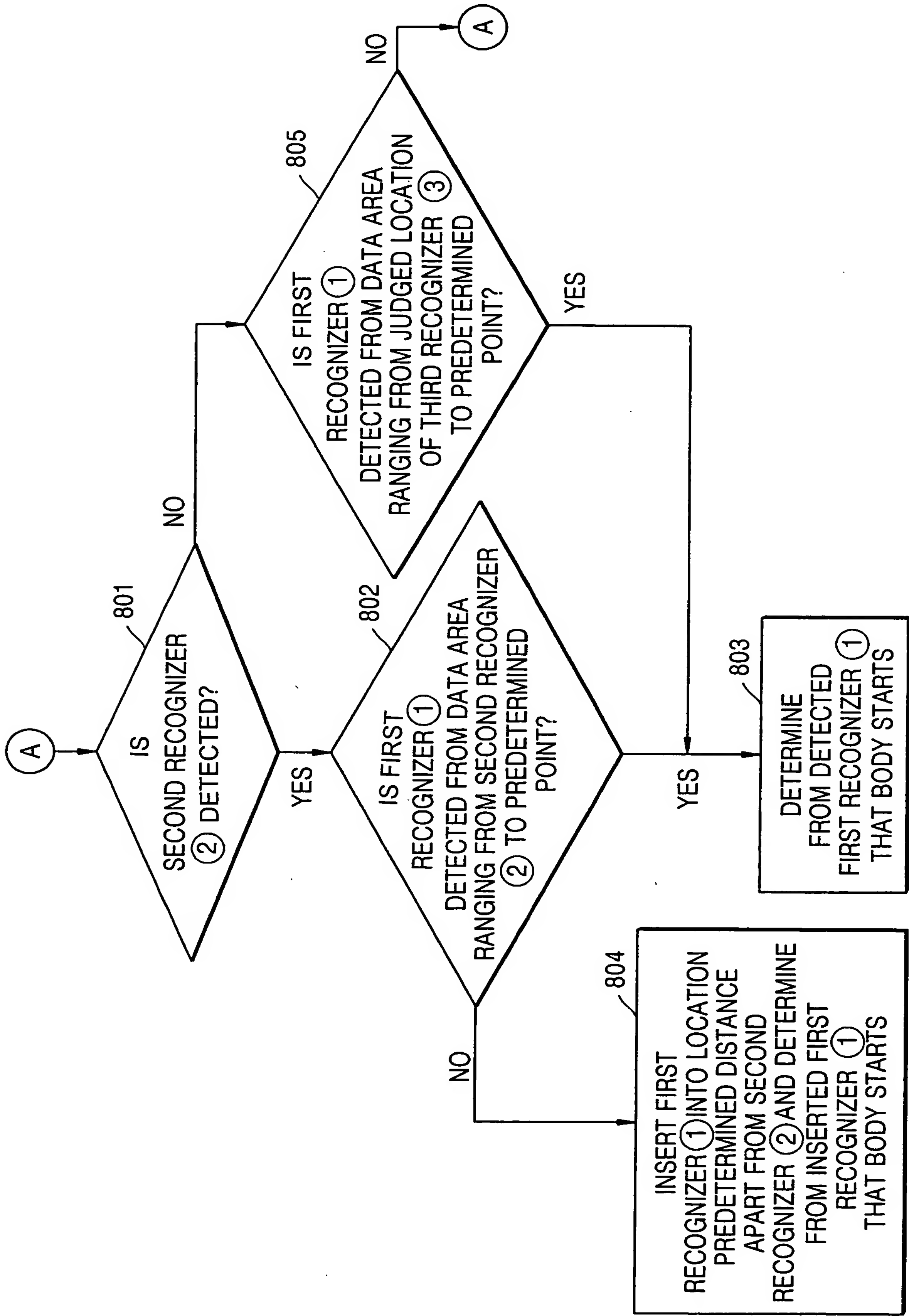


FIG. 9

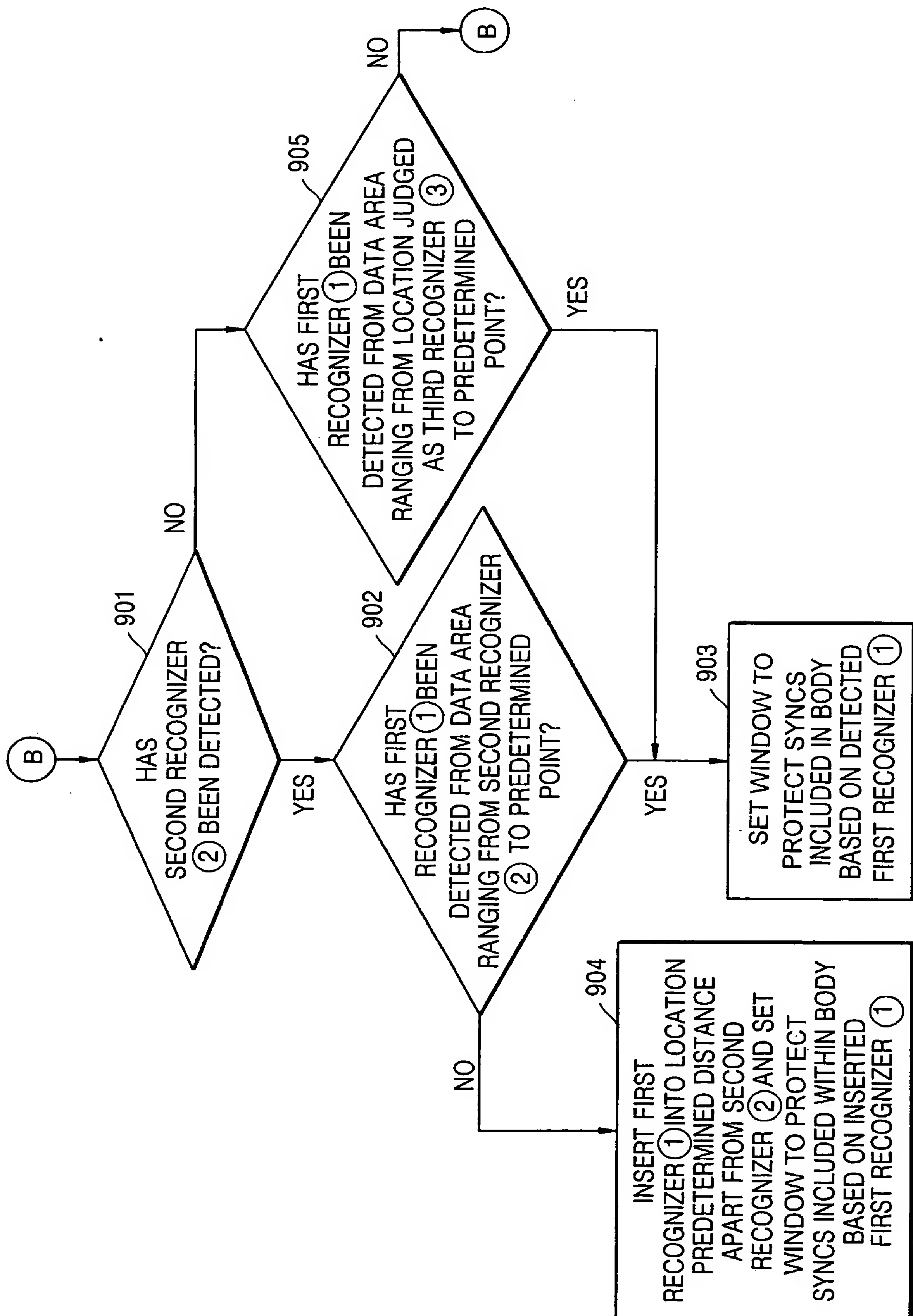


FIG. 10

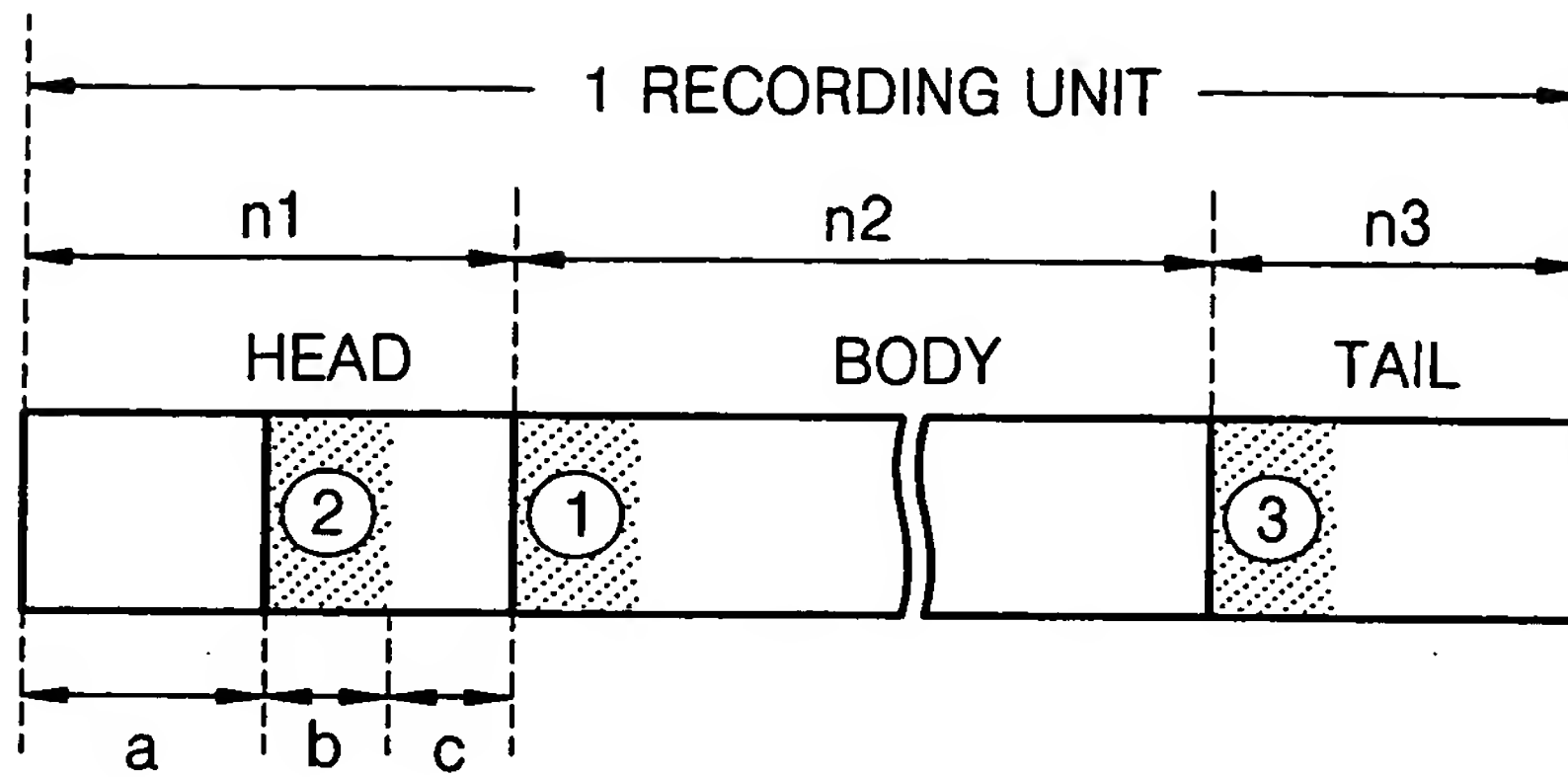


FIG. 11

010001000100....01000100010000000000001000000000001000100010001<ECC Sync>

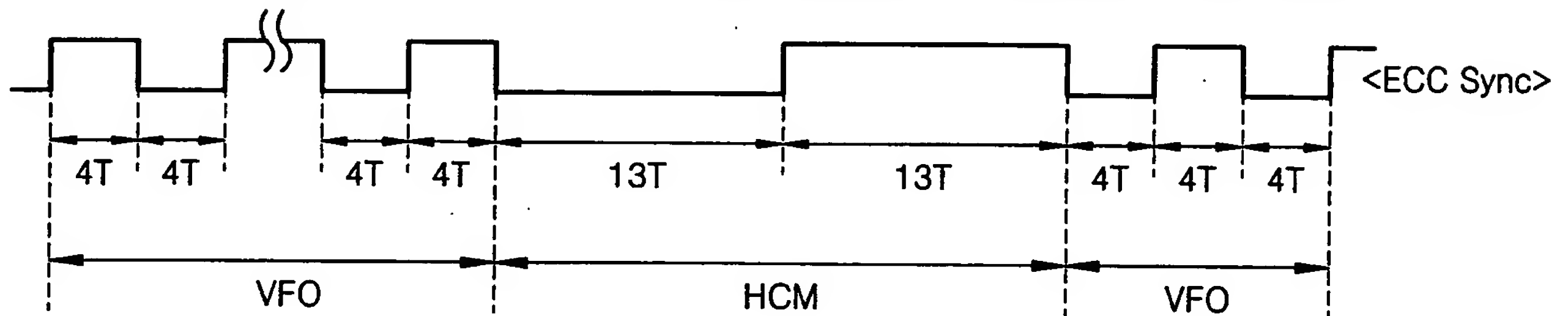


FIG. 12

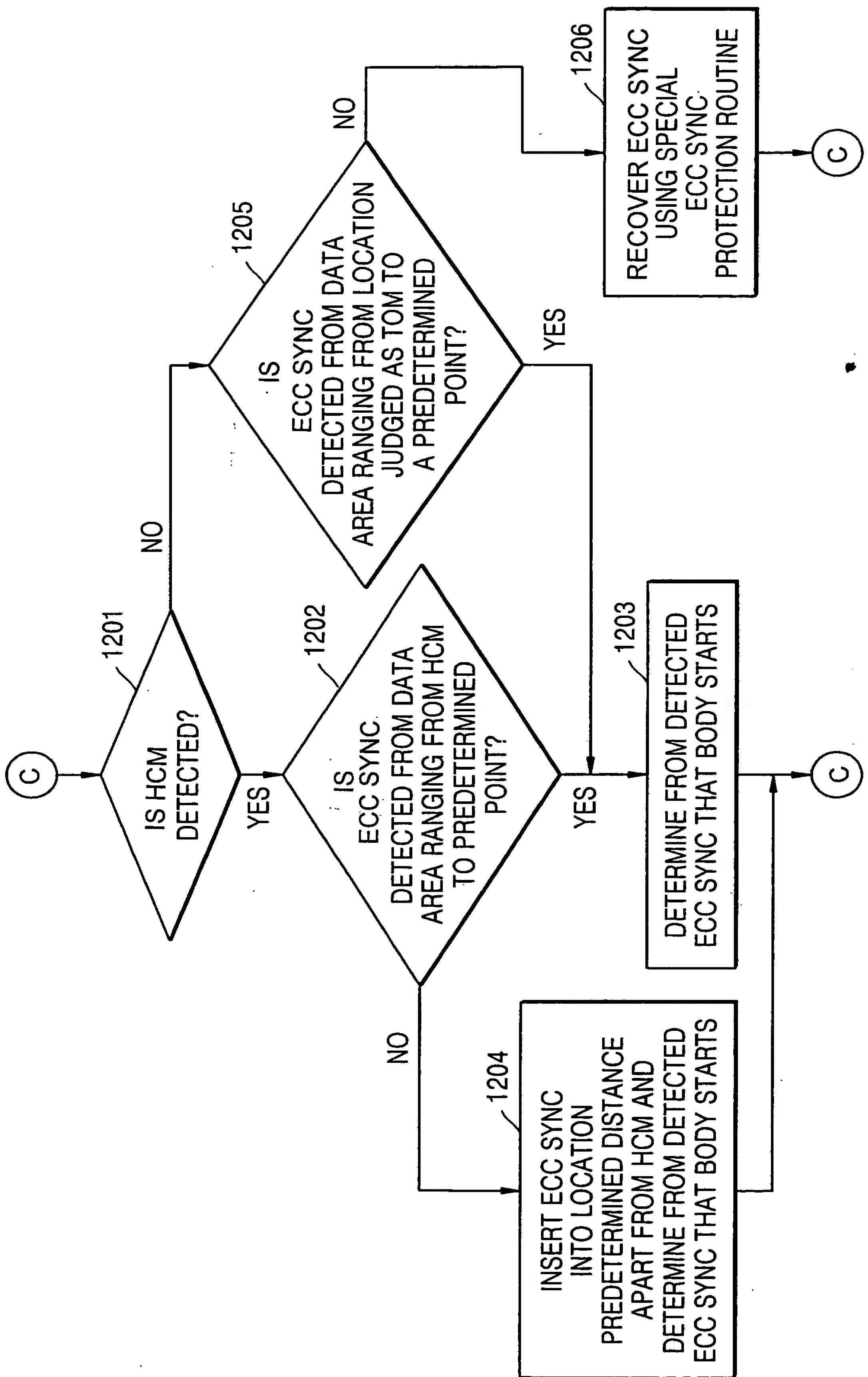


FIG. 13

